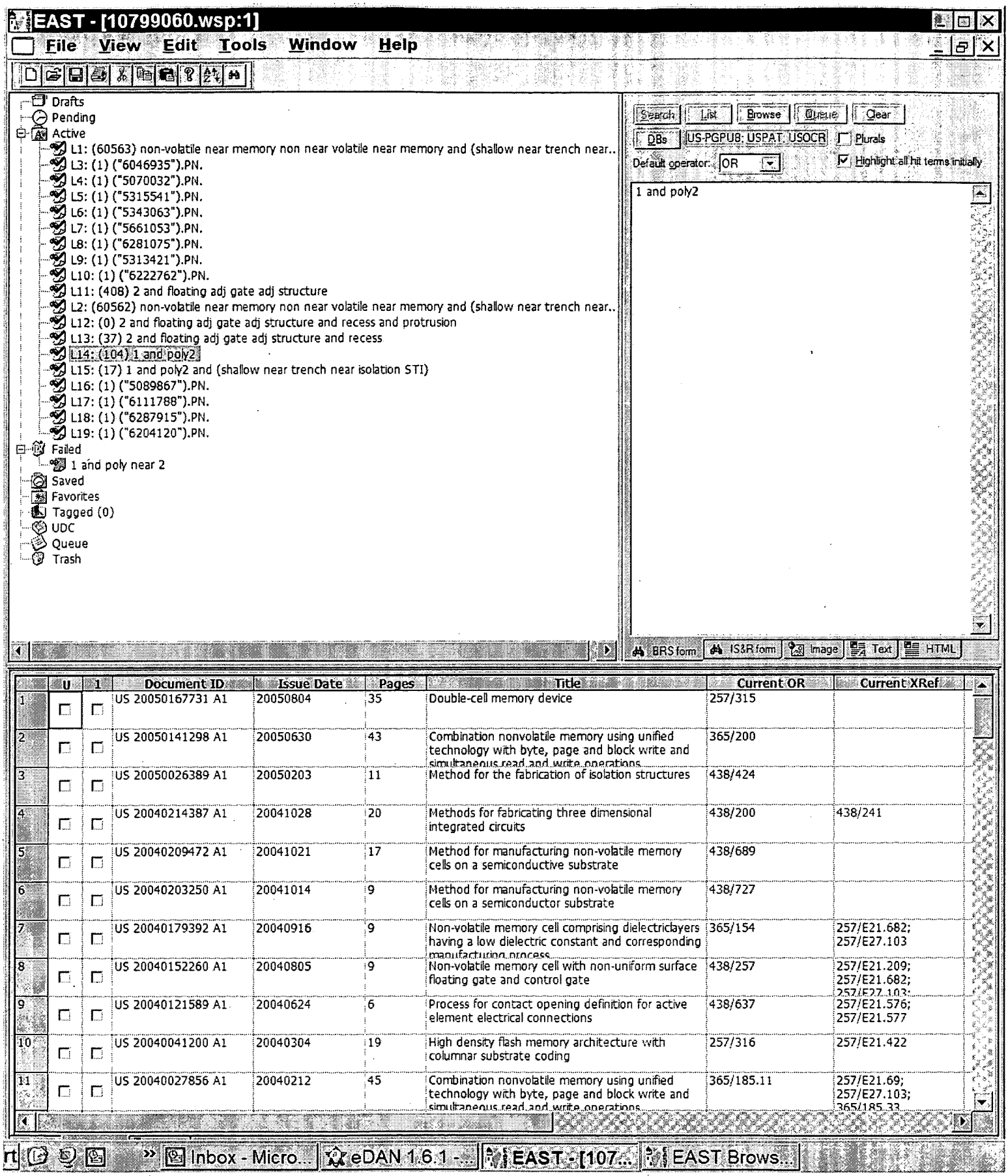

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 20050167731 A1	20050804	35	Double-cell memory device	257/315	
2	☐	☐	US 20050141298 A1	20050630	43	Combination nonvolatile memory using unified technology with byte, page and block write and simultaneous read and write operations	365/200	
3	☐	☐	US 20050026389 A1	20050203	11	Method for the fabrication of isolation structures	438/424	
4	☐	☐	US 20040214387 A1	20041028	20	Methods for fabricating three dimensional integrated circuits	438/200	438/241
5	☐	☐	US 20040209472 A1	20041021	17	Method for manufacturing non-volatile memory cells on a semiconductive substrate	438/689	
6	☐	☐	US 20040203250 A1	20041014	9	Method for manufacturing non-volatile memory cells on a semiconductor substrate	438/727	
7	☐	☐	US 20040179392 A1	20040916	9	Non-volatile memory cell comprising dielectriclayers having a low dielectric constant and corresponding manufacturing process	365/154	257/E21.682; 257/E27.103
8	☐	☐	US 20040152260 A1	20040805	9	Non-volatile memory cell with non-uniform surface floating gate and control gate	438/257	257/E21.209; 257/E21.682; 257/E27.103;
9	☐	☐	US 20040121589 A1	20040624	6	Process for contact opening definition for active element electrical connections	438/637	257/E21.576; 257/E21.577
10	☐	☐	US 20040041200 A1	20040304	19	High density flash memory architecture with columnar substrate coding	257/316	257/E21.422
11	☐	☐	US 20040027856 A1	20040212	45	Combination nonvolatile memory using unified technology with byte, page and block write and simultaneous read and write operations	365/185.11	257/E21.69; 257/E27.103; 365/185.33